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Combinational Logic Circuits Design Using Reversible Logic Gate

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ABSTRACT: Reversible logic has received nice importance within the recent years thanks to its feature of reduction in power dissipation. sizable amount of researches is presently in progress on serial and combinatory circuits exploitation reversible logic. Adder area unit one amongst the foremost necessary circuits utilized in combinatory logic. completely different approaches are planned for his or her style.

KEYWORDS: Reversible logic, decoder

I. INTRODUCTION

Over the previous couple of years, reversible logic has been extensively employed in applied science. In reversible logic bit loss is recovered by distinctive input-output mapping wherever in standard logic it's impracticable. it's one in all distinct feature of reversible logic. In reversible logic the input pattern is recovered from its output pattern however it fails standard logic. In 1961, the analysis of energy dissipated for each info bit loss is a minimum of kTln2 joules, wherever k is physicist Constant and T is temperature at that system operation is performed. the number of energy that is dissipated thanks to one bit data loss is extremely little. however in high speed machine works the amount of knowledge bits is a lot of. Then the warmth dissipation is additionally a lot of. This dissipation affects the performance and reduces the period of system. Bennet incontestable that kTln2 energy won't be dissipated if the inputs are ready to live through its output.Hence the facility dissipation is zero if a network contains solely reversible logic gates. The improvement parameters for the synthesis of reversible logic circuit are

1. Minimum range of gate
2. Minimum quantum value
3. Minimum range of constant inputs
4. Minimum range of garbage outputs
5. Minimum delay

Addition is one amongst the essential operations in multiplication and division algorithms. It plays an important role in several applications like DSP processors, Microprocessors and in computing devices. Hence, it's needed to style quick adder. This paper presents a completely unique style of reversible optimized fault tolerant Full adder/ Full subtractor. This paper proposes associate degree economical approach to implement 1-bit adder which can play an important role in future quantum computers.

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II. BASIC REVERSIBLE GATES

Reversible gate may be a digital circuit whose variety of inputs and variety of outputs area unit equal. If there are unit k inputs, there'll be k outputs. Every input pattern has distinctive output pattern. This is often referred to as one-one correspondence.

There are several reversible gates offered in literature. Among them few necessary gates area unit Richard Feynman Gate (FG), Richard Feynman Double Gate (F2G), Fred kin Gate (FRG), Toffoli Gate (TG), and Peres Gate (PG).

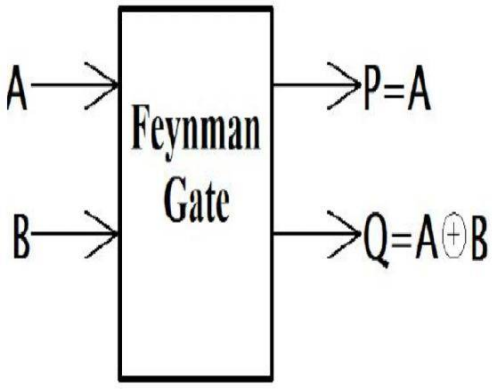
A. FEYNMAN GATE

Feynman gate is one among the fundamental reversible logic gates with a pair of inputs and a couple of outputs, conjointly known as 2*2 gates. The inputs square measure denoted by I (A, B) and also the outputs square measure denoted by O (P, Q). The outputs square measure given by

$$P = A ; Q = A \oplus B ;$$

TRUTH TABLE OF FEYNMAN GATE

Inputs		Outputs	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0



Feynman gate

Feynman gate is called as a copying gate.

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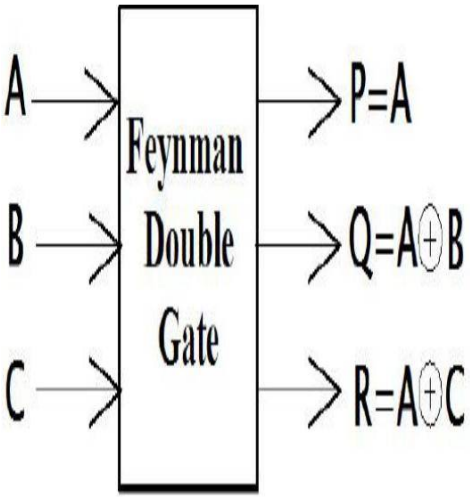
B. FEYNMAN DOUBLE GATE

Feynman Double gate additionally |is additionally one amongst the fundamental reversible computer circuit with three inputs and three outputs also depicted as 3*3 gates. The inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, R).The relation between inputs and outputs are given by

$$P = A; Q = A \oplus B; R = A \oplus C;$$

TRUTH TABLE OF DOUBLE FEYNMAN GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0



Feynman Double gate

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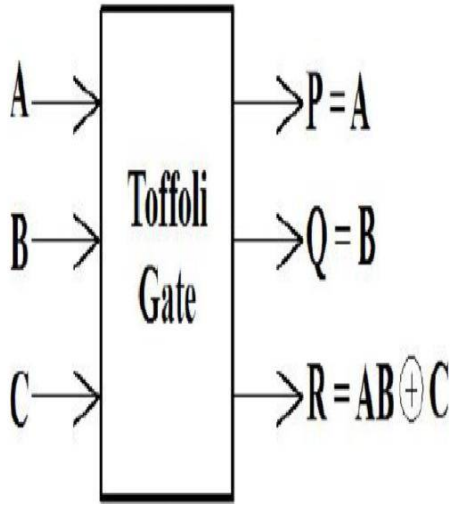
C. TOFFOLI GATE

Toffoli gate is additionally one among the fundamental reversible logic gates with three inputs and three outputs. It additionally known as as 3*3 gates. For a toffoli gate, the inputs square measure denoted by I (A, B, C) and outputs square measure denoted by O (P, Q, R).The relationship between inputs and outputs is

TRUTH TABLE OF TOFFOLI GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0



Toffoli gate

P = A ; Q = B ; R = AB ⊕ C ;

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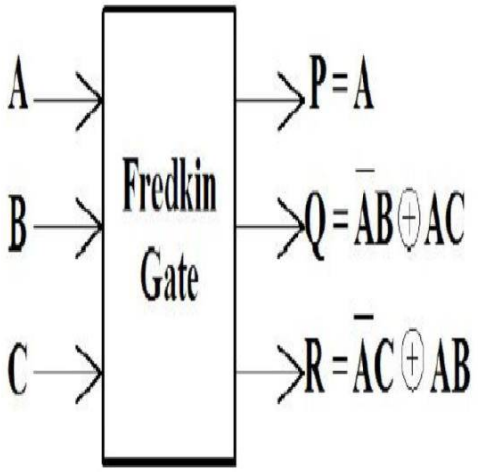
D. FREDKIN GATE

Fredkin gate is additionally one in all the essential gate of reversible computer circuit with three inputs and three outputs and denoted by 3*3 gates. The inputs are denoted by I (A, B, C) and outputs are denoted by O (P, Q, and R). The connection between inputs and outputs is given by

TRUTH TABLE OF FREDKIN GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1



Fredkin Gate

P = A ; Q = $\bar{A}$B ⊕ AC ; R = $\bar{A}$C ⊕ AB ;

For Fredkin gate the quantum cost is 5.

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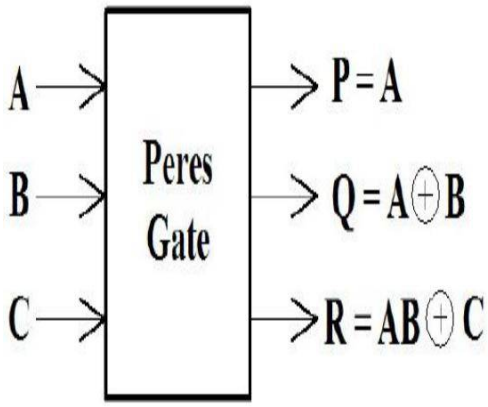
E. PERES GATE

Peres gate conjointly is additionally one among the fundamental reversible computer circuit with three inputs and three outputs also denoted as 3*3 gates.

TRUTH TABLE OF PERES GATE

Inputs			Outputs		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0



Peres Gate

The inputs square measure denoted by I (A, B,C) and outputs square measure denoted by O(P, Q, R). The link between inputs and outputs is given by

P = A ; Q = A ⊕ B ; R = AB ⊕ C ;

III. PROPOSED WORK

In every digital circuit the basic components are N-Bit Adders and N-Bit Multipliers. In the above said components the basic element is 1-Bit Adder. If we worked to implement 1- Bit Adder efficiently then it indirectly

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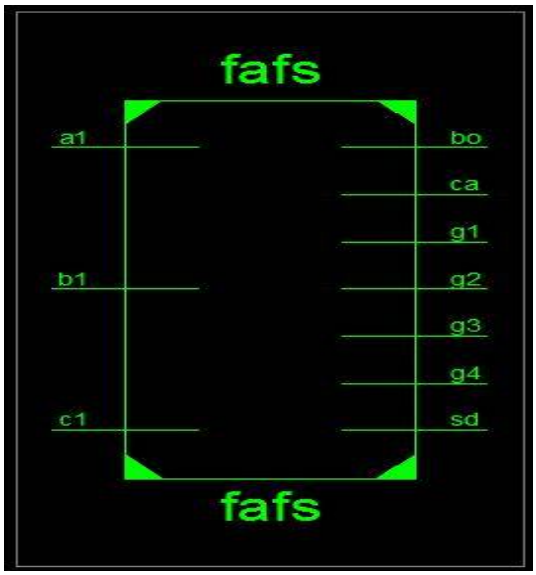
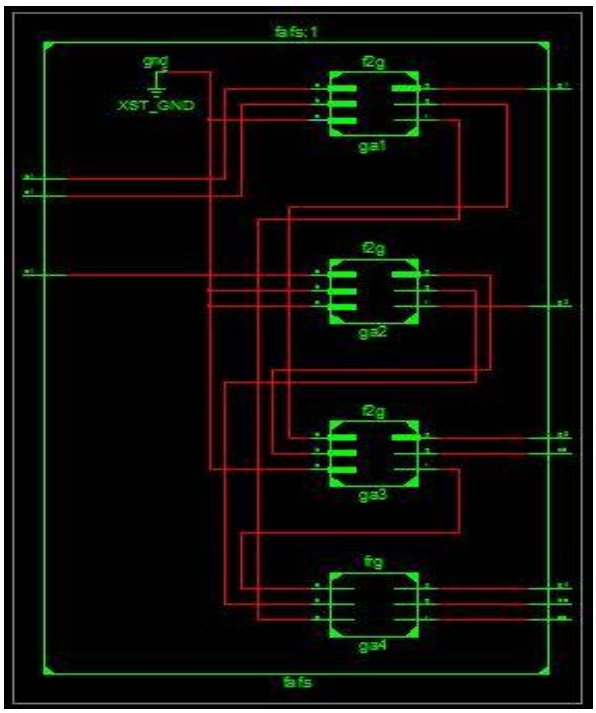
helps for the optimistic design of any Digital circuit. This paper proposes a circuit which works as a Full Adder and full Subtractor.



2 outputs. In the 3 input bits 2 bits are data bits and other bit is present stage borrow. The 3 input variables are denoted by A, B and Cin(for convenience purpose present stage borrow is denoted by Cin).



Full Adder and Full Subtractor

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A full adder is a combinational circuit that adds 3 input bits and produces 2 outputs. In the 3 input bits 2 bits are data bits and other bit is previous stage carry. The 3 input variables are denoted by A, B and Cin. The outputs sum and carry are denoted by 'S' and 'Cout'. The mathematical equation representing the full adder is A+B+Cin. A full subtractor is a combinational circuit that subtracts 2 input bits from first input and produces

RTL Schematic

The outputs Difference and Borrow are denoted by 'D' and 'Bout'. The mathematical equation represents full subtractor is A-B-Cin. The boolean expressions of Full Adder / Full Subtractor are
Sum / Difference = A ⊕ B ⊕Cin Carry out
Carry out (Cout) = (A ⊕ B)Cin⊕ AB
Borrow out (Bout) = (A B)Cin⊕ 'AB

IV. CONCLUSION

This method focus mainly on implementation of a model which can be operated as full adder as well as full subtractor with better performance. Here a structure is proposed with parity preserving gates which reduce testing hardware. The reversible logic concept work efficiently if number of garbage outputs, constant inputs and quantum cost is low. The power dissipation is zero if the reversible logic circuits are implemented with quantum gates. If we do that then we can save power, money as well as nature.

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